Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A memory package comprising:

a first cover portion;

a first electronics sub-assembly that comprises a circuit board with at least one memory module socket and at least one controller chip, wherein said first electronics assembly is supported by said first cover portion;

a second cover portion connected to said first cover portion; and

a second electronics sub-assembly that comprises a circuit board with at least one memory module socket and at least one controller chip, wherein said second electronics assembly is supported by said second cover portion; wherein

said first and second cover portions are moveable between a closed position wherein said electronics sub-assemblies are nested such that a memory module socket mounted to the first circuit board is adjacent to a controller chip mounted to the second circuit board and a memory module socket mounted to the second circuit board is adjacent to a controller chip mounted to the first circuit board.

2. (Original) The memory package of claim 1 wherein each of said first and second cover portions further comprises a base surface; and wherein when said cover portions are in the closed position, the base surfaces of said cover portions face each other.

3. (Original) The memory package of claim 1 wherein the circuit boards of said first and second electronics sub-assemblies are positioned substantially

parallel to and offset from each other when said first and second cover portions are in the closed position.

4. (Cancelled).

5. (Original) The memory package of claim 1 wherein each of said first and second cover portions further comprises a base surface; and wherein when said cover portions have an open position wherein the base surfaces of said cover portions do not face each other.

6. (Original) The memory package of claim 5 wherein the circuit boards of said first and second electronics sub-assemblies are positioned substantially parallel to and substantially co-planar with each other when said first and second cover portions are in the open position.

7. (Original) The memory package of claim 1 further comprising a hinge pivotally connecting said first cover portion and said second cover portion.

8. (Original) The memory package of claim 1 further comprising a latch operable to retain said cover portions in the closed position.

9. (Original) The memory package of claim 1 wherein further comprising an electrical connector operable to couple said electronic sub-assemblies to a processor-based device.

10. (Original) The memory package of claim 1 wherein each electronic sub-assembly further comprises an electrical connector operable to couple one electronic sub-assembly to a processor-based device.

11. (Original) The memory package of claim 1 further comprising a handling aperture in at least one of said cover portions.

12. (Original) The memory package of claim 1 wherein the circuit board of said first electronics assembly is identical to the circuit board of said second electronics assembly.

13. (Original) The memory package of claim 1 further comprising a plurality of memory modules received by the memory module sockets.

14. (Currently amended) A computer system comprising:
a processor;
a chassis supporting said processor; and
a memory package comprising;
an electronics assembly comprising first and second circuit boards, wherein each circuit board is coupled to at least one memory module and at least one memory controller; and
a housing assembly supporting said electronics assembly, wherein said housing assembly has a first cover portion supporting the first circuit board and a second cover portion supporting the second circuit board;
wherein said memory package has a closed position and an open position, wherein in the closed position the memory modules mounted to said first circuit board are adjacent to the memory controller mounted to the second circuit board, the memory modules mounted to the second circuit board are adjacent to the memory controller mounted to the first circuit board, said housing engages said chassis, and said electronics assembly electrically couples with said processor.

15. (Original) The computer system of claim 14 wherein the first and second circuit boards are positioned substantially parallel to and offset from each other when said memory package is in the closed position.

16. (Cancelled).

17. (Original) The computer system of claim 14 wherein said memory package has an open position wherein said housing is disengaged from said chassis and said electronics assembly is decoupled from said processor.

18. (Original) The computer system of claim 17 wherein the first and second circuit boards are positioned substantially parallel to and substantially co-planar with each other when said memory package is in the closed position.

19. (Original) The computer system of claim 14 wherein the electronics assembly further comprises at least one electrical connector coupled to the first and second circuit boards, wherein the at least one electrical connector couples the electronics assembly to said processor.

20. (Original) The computer system of claim 14 wherein the housing assembly further comprises a hinge pivotally connecting the first cover portion and the second cover portion.

21. (Original) The computer system of claim 14 wherein the housing assembly further comprises a latch operable to retain said cover portions in the closed position.

22. (Currently amended) A memory package comprising:

means for housing a first and second electronics sub-assemblies, wherein each sub-assembly has at least one memory module and at least one memory controller chip mounted thereto;

means for moving at least a portion of said means for housing between an open position allowing access to the memory modules and a closed position where the two electronics sub-assemblies are nested together such that a memory module mounted to the first electronic

sub-assembly is adjacent to a memory controller chip mounted to the second electronic sub-assembly and a memory module mounted to the second electronic sub-assembly is adjacent to a memory controller chip mounted to the first electronic sub-assembly.

23. (Original) The memory package of claim 22 further comprising means for coupling the first and second electronics sub-assemblies to a processor-based device when said means for housing is in the closed position.

24. (Original) The memory package of claim 22 further comprising means for retaining said means for housing in the closed position.